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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,411	11/14/2003	Adam H. Leventhal	03226.346001; SUN040247	6947

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EXAMINER	
VO, TED T	
ART UNIT	**PAPER NUMBER**
2191	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,411	LEVENTHAL ET AL.	
	Examiner	Art Unit	
	Ted T. Vo	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11/14/03 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 3/15/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the communication filed on 11/14/2003.

Claims 1-20 are pending in the application.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Omum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-20 are provisionally rejected on the ground of nonstatutory double patenting over claims 1-16 of copending Application No. **10/713,409, available in the** Attorney Docket Number: **03226.347001; SUN040249.** This is a provisional double patenting rejection since the conflicting claims have not yet been patented. The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: Claims 1-16 of the US patent application serial No. **10/713,409** has all claimed subject matters presenting in the instant claims 1-20. Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Tamches, "Fine-Grained Dynamic Instrumentation of Commodity Operating System Kernels", University of Wisconsin, 2001.

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per claim 1:Tamches discloses, **A method for tracing an instrumented program, comprising:**

triggering a probe in the instrumented program (See p. 49, instrument point, e.g. encountering the instrumentation point – See further IBM Dprobes, p. 15, or see p.62, sec. 4.5.1, "entry point");

obtaining an original instruction associated with the probe (See p. 49,code patch and instrument point, or see p. 62, "unconditional branch" in Original Function);

loading the original instruction into a scratch space (See Figure 3.1, p. 27, Code Patch for privileged user programs and kernel modules is attached into a kernel address space, or see p. 62, Springboard: "*scratch space*"); **and**

executing the original instruction in the scratch space using the thread (the patch code is executed at boot time or run-time of the kernel, or the execution in the springboard), **wherein**

executing the original instruction results in placing the instrumented program in a state equivalent to natively executing the original instruction (See Figure 4.1, the statement in the description of Code Patch: Overwritten instruction or equivalent sequence, or see p. 62, the execution of New Version of Function).

As per claim 2:Tamches discloses, **The method of claim 1, further comprising:**

emulating a location dependent instruction to determine a value of a program counter if the original instruction is a control-flow instruction wherein semantics of the location dependent instruction depend on a location of the original instruction within the instrumented program (i.e., see sec. 4.2.1, p.51- 52) .

As per claim 3:Tamches discloses, **The method of claim 1, further comprising:**

incrementing a value of a program counter using a size of the original instruction (see p. 71, e.g., event counter, etc., see p. 72, Figure 5.1, or the increment of program counter during the execution of the Original function in p. 62).

As per claim 4:Tamches discloses, **The method of claim 1, further comprising:**

determining a value of a program counter; and

loading the value of the program counter into the scratch space (P. 58, see sec. 4.3.3, particularly, see Figure 4.7. instrument point contain the address of code patch. Note "springboard" is scratch space. The mechanism of Figure 4.9, p. 62, reads the limitation).

As per claim 5: Tamches discloses, **The method of claim 4, wherein determining the value of the program counter comprises:**

incrementing the value of the program counter using a size of the original instruction if the original instruction is not a control-flow instruction; and

emulating a location dependent instruction to determine the value of the program counter if the original instruction is a control-flow instruction (see sec. 4; particularly, see the mechanisms of Figure 4.7, p. 58, and Figure 4.9, p. 62: *is/ is not a control-flow instruction*).

As per claim 6: Tamches discloses, **The method of claim 1, furthering comprising:**

loading a control transfer instruction into the scratch space prior to executing the original instruction (See sec. 3.3.2, p. 30, handling control-flow instructions; see Figure 3.3, p. 33; see Figure 4.1, p. 49, Figure 4.7, p. 58, and Figure 4.9, p. 62).

As per claim 7: Tamches discloses, **The method of claim 6, wherein the control transfer instruction includes a value of a program counter** (See sec. 3.3.2, p. 30, handling control-flow instructions; see Figure 3.3, p. 33).

As per claim 8: Tamches discloses, **The method of claim 1, wherein the probe corresponds to a trap** (See discussion of trap instruction in p. 15-17; and of the SPARC in p. 40, see trap handler used in splicing, p. 66).

As per claim 9: Tamches discloses, **The method of claim 1, wherein obtaining the original instruction comprises:**

searching a look-up table using a program counter value, wherein the look-up table comprises the original instruction associated with the probe and an address associated with the original instruction (See sec. 4.6.1, p.66-67; the trap handler using hash table as loop up address).

As per claim 10: Tamches discloses, **The method of claim 1, wherein the scratch space is allocated on a per-thread basis** (The kernel's instrumentation discussed by Tamches, particularly, the SPARC platform, supports single-stepped /single-multiple thread – See whole reference).

As per claim 11: Tamches discloses, **The method of claim 1, wherein the instrumented program is executed on multi-thread architecture** (The kernel's instrumentation discussed by Tamches, particularly, the SPARC platform, supports single-stepped /single-multiple thread – See whole reference).

As per claim 12: Tamches discloses, **The method of claim 1, wherein executing the original instruction comprises single-stepping the original instruction** (The kernel's instrumentation discussed by Tamches, particularly, the SPARC platform, supports single-stepped /single-multiple thread – See whole reference).

As per Claim 13: Tamches discloses,

A system for tracing an instrumented program, comprising:

a thread configured to execute the instrumented program (P. 27, Figure 3.1, e.g., Instrumentation request and kerninstd);

a look-up table arranged to store an address and a corresponding original instruction (See sec. 4.6.1, p.66-67; the trap handler using hash table as loop up address);

a trap handler configured to halt execution of the thread when a trap instruction is encountered and using an address of the trap instruction to obtain the corresponding original

instruction from the look-up table (See discussion of trap instruction in p. 15-17; and of the SPARC in p. 40, see trap handler used in splicing, p. 66);

a scratch space arranged to store the original instruction (Available address space in kernel such as seen in p. 27, Figure 3.1, or "springboard in Figure 4.7, p. 58, Figure 4.9, p. 62); **and**

an execution facility for executing the original instruction to obtain data (the Figure 3.1, or Figure 4.7, Figure 4.9).

As per Claim 14: Tamches discloses, *The system of claim 13, further comprising: a buffer for storing the data* (such as I-cache, or the kernel space as seen in Figure 3.1, or Figure 4.7, Figure 4.9).

As per Claim 15: Tamches discloses, *The system of claim 13, further comprising:*

a tracing framework emulating a location dependent instruction to determine a value of a program counter if the original instruction is a control-flow instruction (i.e., Figures 4.7, 4.9 in section 4).

As per Claim 16: Tamches discloses, *The system to claim 13, wherein the trap handler sets the value of the program counter to the value of a next address immediately the address of the trap instruction after executing the original instruction* (see sec. 4.6.1, p.66-67).

As per Claim 17: Tamches discloses, *The system of claim 13, wherein the trap handler increments a value of a program counter using a size of the original instruction if the original instruction is not a control-flow instruction* (see p. 71, e.g., event counter, etc., see p. 72, Figure 5.1, or the increment of program counter during the execution of the Original function in p. 62).

As per Claims 18-20: See rationale addressed in Claims 10-12 above.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708.

The facsimile number for the organization where this application or proceeding is assigned is the Central Facsimile number **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TTV
February 16, 2007

TED VO
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100